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1×*M* Packet-Switched Router Based on the PPM Header Address for All-optical WDM Networks

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ABSTRACT

This paper presents an all-optical 1×*M* router architecture for simultaneous multiple-wavelength packet routing, without the need for wavelength conversion. The packet header address is based on the pulse position modulation (PPM) format, which allows the use of only a single-bitwise optical AND gate for fast packet header address correlation. The proposed scheme offers both multicast and broadcast capabilities. We've demonstrated a high speed packet routing at 160 Gb/s in simulation, with a low channel crosstalk (CXT) of ~ -27 dB with a channel spacing of > 0.4 THz and a demultiplexer bandwidth of 500 GHz. The output transfer function of the PPM header processing (PPM-HP) module is also investigated in this paper.

Keywords

Wavelength division multiplexing, packet switching, pulse position modulation, address correlation, symmetric Mach-Zehnder, optical switch.

1. INTRODUCTION

The ever increasing demand for a high speed Internet access together with a high definition digital video broadcasting (video-on-demand) requires an ultrahigh speed networking from the source to the end users. Current networks based on a combination of optical fibre links, radio frequency links and twisted pair cables suffers from the speed bottleneck mainly imposed by the non-optical links. Thus the logical way forward would be to do away with all non-optical components and links as much as possible. An end-to-end all-optical packet switched network [1, 2] would offer speed, flexibility, lower power consumption and has the capability to deal with the bursty traffic. However, to be able to fully utilize this promising potential of such networks, the packet header processing (including clock recovery and packet address correlation) and routing decision would have to be performed in the optical domain rather than in the electrical domain, to avoid the speed bottleneck imposed by the slow response of existing electronic devices. In [3-5] ultra high-speed Boolean logic gates including AND, OR and XOR operating above 40 Gb/s have been reported as the key enabling technology for realising all optical routers. Currently the dominant technique for optical packet header processing is based on the sequential correlation of the incoming packet header address with all entries of a routing table within each node. This method is most viable for a small size network with a reasonable size routing table both in terms of processing speed and implementation complexity. However, for a large size network with a routing table of hundreds or thousands of entries may

no longer be attractive because of the complexity and increased packet header processing time. The latter will lead to a noticeable increase in the packet processing time at every router, which could be significantly reduced by a non-conventional signal formatting. In [6], an alternative packer header processing scheme known as the PPM-HP has been proposed to reduce the processing time by converting both the header address and the routing table entries from a return-to-zero (RZ) format to a PPM format for a single wavelength routing network. In this paper, we introduce the PPM-HP concept to the wavelength division multiplexed (WDM) all-optical router for a number of reason including: (i) a significantly reduced size routing table with each multiple PPM pulses per entry, (ii) significantly simplified packet header address correlators (using just one bitwise AND gate in place of a large number of gates), thus leading to significantly reduced processing time, (iii) offering unicast, multi-cast and broadcast capabilities embedded in the optical layer, and (iv) reduced complexity requiring no PPM address conversion module as in [7], no wavelength conversion [8-10] and all-optical flip-flops modules [11, 12].

The paper is organized as follows: after introduction, the correlation principle as well the PPM-HP node architecture is outlined in Section 2. The WDM router architecture incorporating PPM header address format is described in Section 3. The simulation results, output packet intensity fluctuation and inter-channel crosstalk performance, and the output transfer function of the PPM-HP module versus different values of input power are also investigated and discussed in Section 4. Finally, Section 5 will conclude the paper.

2. PPM ROUTING TABLE (PPRT)

A typical packet is composed of a header and the payload bits. The header contains both the clock, normally one bit and is used for synchronization within the router, and the address bits. In [6] PPM is adopted for both the header address and the routing table entries as an alternative to the conventional non-return-to-zero (NRZ) and RZ signal formats [7]. A PPM

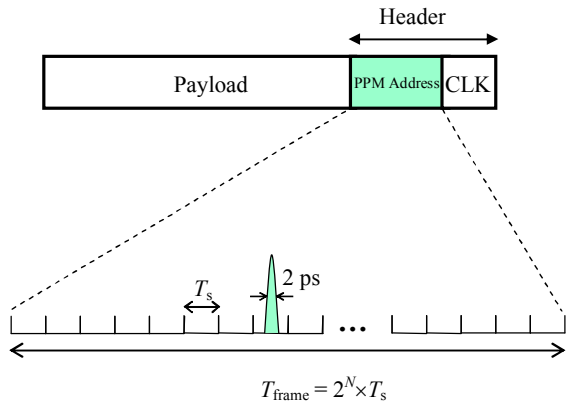


Figure 1. An optical packet with the PPM header address

header address symbol is composed of 2^N time slots T_s where N is the input address bit resolution with a pulse of duration $\leq T_s$. The position of the pulse corresponds to the target address decimal metric, see Figure 1. For example, a target address of "0011" with a decimal value of 3 is represented in a PPM format as "0001000000000000". In [6].it has been shown that a router employing PPM formatted address and routing table entries greatly reduced the header address correlation time compared to the conventional routing tables (CRT). Table 1

Table 1. The conventional and PPM based routing tables

Address patterns (N=4)	Output Port (M=3)	PPRT entries with 16 slots
0 0 0 0 0 0 0 1 0 1 0 0 1 0 0 1 1 0 1 1 1 1 1 1	**1**	E_1 Decimal values 0 1 4 9 11 15 PPM pulses
0 0 0 0 0 0 1 0 0 1 1 0 0 1 1 1 1 1 0 1 1 1 1 0	**2**	E_2 Decimal values 0 2 6 7 13 14 PPM pulses
0 0 0 0 0 0 0 1 0 0 1 1 0 1 0 1 1 0 0 0 1 0 1 0 1 1 0 0	**3**	E_3 Decimal values 0 1 3 5 8 10 12 PPM pulses

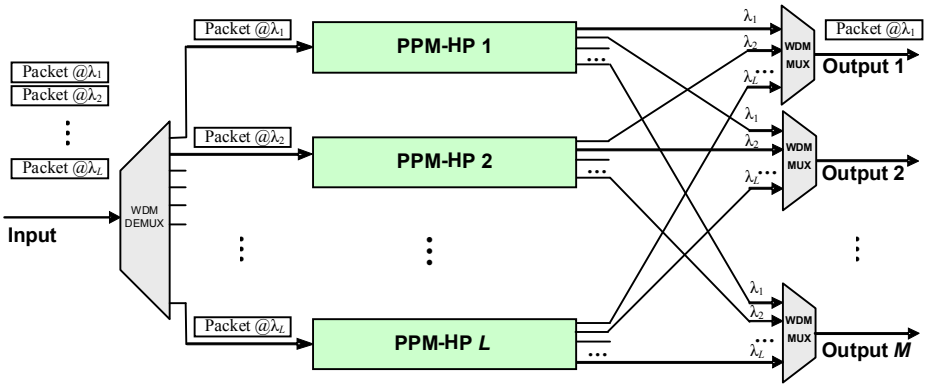


Figure 2. The WDM router architecture for $L = 2$ and $M = 3$

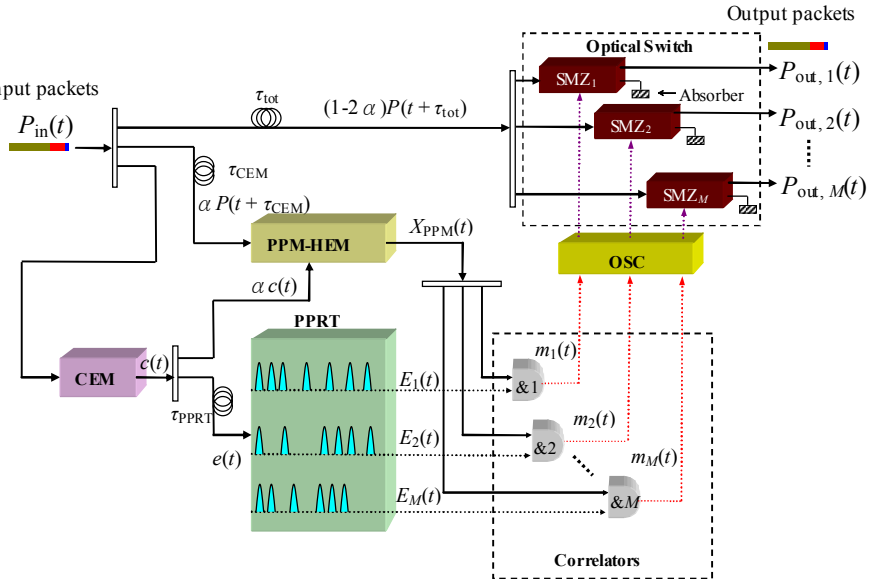


Figure 3. The schematic diagram of PPM-HP

illustrates a routing table for a traditional 4-bit binary address, where 16 possible addresses are grouped into M groups based on the intended target output ports. Here $M = 3$ representing the number of output ports. The 3rd column shows the PPRT entries E_m ($m = 1,2,...M$) of length $2^N \times T_s$ for each group. Note that the number of entries is reduced from 16 to 3 compared to the CRT, thus resulting in a reduced header address correlation time. A packet header address matching one or more patterns in a group can be switched to more than one output ports. At a very high bit rate R_b (in this case 160 Gb/s) generating an ultra short PPM pulse is a challenging task, therefore here we have kept the pulse duration $T_s = T_b = 6.25$ ps.

3. WDM ROUTER ARCHITECTURE

Figure 2 depicts a block diagram of a $1\times M$ WDM router architecture composed of a $1\times L$ demultiplexer, L PPM-HPs, and M $L\times 1$ multiplexers, where L is the number of wavelengths. The incoming WDM packets at multiple-wavelengths (λ_1, λ_2 … and λ_L) are applied to a bank of PPM-HP modules via a WDM demultiplexer. Packets at

specific wavelengths are processed at the PPM-HP modules before being broadcasted to all $L\times1$ multiplexers. In contrast to existing schemes this architecture uses fewer number of laser sources since there is no requirement for the wavelength conversion modules. Figure 3 illustrates a schematic block diagram of $1\times M$ PPM-HP module, which is composed of an asynchronous clock extraction module (CEM), a PPM header address extraction module (PPM-HEM)**,** a PPRT, AND gates, fibre delay lines (FDLs), symmetric Mach-Zehnder based all-optical switches (OS), and an OS control module (OSC). The incoming optical packet $P_{in}(t)_{\lambda i}$ is applied via 1×3 splitter to the CEM, PPM-HEM and OS with the delays of 0, τ_{CEM} (required time for the clock extraction) and τ_{tot} (total required time for PPM address correlation), respectively. τ_{CEM} and τ_{tot} are the delays required for clock extraction and PPM address correlation, respectively. The CEM, PPM-HEM and PPRT modules configurations are the same as those adopted in [6]. The extracted clock signal $c(t)$ and its delayed version $\alpha c(t - \tau_{PPRT})$ are applied to the PPM-HEM and PPRT modules, respectively, where α is the 1×3 splitting coefficient. PPRT is constructed by applying the delayed clock signal through a number of FDLs as in [6]. The packet header address, in PPM format, at the output of the PPM-HEM is correlated with the PPRT entries using a bank of all-optical AND gates. The correlated output pulses are applied to the OS via OSC to ensure the input packet is delivered to its intended output port. If more than one PPM pulse is located at the same position in more than one (or all) PPRT entries, then the input packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

The packet header address correlation time (or header recognition time) for PPRT scheme is given as:

$$T_{\mathrm{PPRT}} = 2^N \times T_{\mathrm{s}} . \qquad (1)$$

In the conventional schemes, packet header recognition is carried out by sequentially correlating the address bits with each individual entries of the routing table. The packet header address recognition time for the CRT scheme is defined as:

$$T_{\mathrm{CRT}} = 2^N \times N \times T_{\mathrm{AND}} \times M^{-1} , \qquad (2)$$

where M is the number of the router's output ports, and T_{AND} is the minimum time interval required for two successive AND operations, which is limited by the SOA recovery time. Typically T_{AND} (hundreds of picoseconds) is much greater than T_b (few picoseconds) in high-speed optical networks (bit-rate > 40 Gb/s).

Comparing with CRT, the correlation-time gain for PPRT is defined as the ratio of the time required for CRT scheme

Table 2. Simulation parameters

Parameters	Values
Data packet bit rate $R_b = 1/T_b$	160 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength 1 (f_1)	1554 nm (193.1
Wavelength 2 (f_2)	1546 nm (194.1
Data pulse widths (FWHM)	2 ps
PPM slot duration T_s (= T_b)	6.25 ps
Average transmitted packet pulse	2 mW
Optical bandwidth of the WDM (de)multiplexers	4 nm (500 GHz)
Splitting factor α	0.25
Number of control pulses	60
Average control pulse power	10 mW
SOA injection current	150 mA
SOA active region length	500×10^{-6} m
SOA active region width	3×10^{-6} m
SOA active region height	80×10^{-9} m
SOA n_{sp}	2
Confinement factor	0.15
Enhancement factor	5
Differential gain	2.78×10^{-20} m^2
Internal loss	40×10^{2} m^{-1}
Recombine constant A	1.43×10^{8} s^{-1}
Recombine constant B	1×10^{-16} m^{3}s^{-1}
Recombine constant C	3×10^{-41} m^{6}s^{-1}
Carrier density at transparency	1.4×10^{24} m^{-3}
Initial carrier density	3×10^{24} m^{-3}

T_{CRT} over the required time for PPRT scheme T_{PPRT}, and is given by:

$$R_{\mathrm{PPRT}} = \frac{N \times T_{\mathrm{AND}}}{M \times T_{\mathrm{s}}} . \quad (3)$$

4. RESULTS AND DISCUSSIONS

The proposed WDM router [13] is simulated by using the Virtual Photonics simulation package (VPI^{TM}). Table 2 outlines all the main simulation parameters. Twelve WDM optical packets with addresses of #0, #1, #3, #6, #9, #14 (in decimal), and #0, #4, #7, #10, #13, #15 are transmitted at wavelengths of λ_1 and λ_2, respectively. Packets are sequentially transmitted at 160 Gb/s with 1 ns inter-packet guard interval. Each packet is composed of a 1-bit clock, a 16-bit PPM address, and a 53-byte payload (ATM cell size) [14]. The total processing time of the all-optical PPM-HP based router τ_{tot} (i.e. the time delay between the input packets and switched packets) in this simulation (N = 4, $T_s = T_b$ = 6.25 ps) is equal to 112.5 ps, which is calculated as follows:

$$\tau_{\mathrm{tot}} = 2^N \times T_{\mathrm{s}} + 2T_{\mathrm{b}}, \quad (4)$$

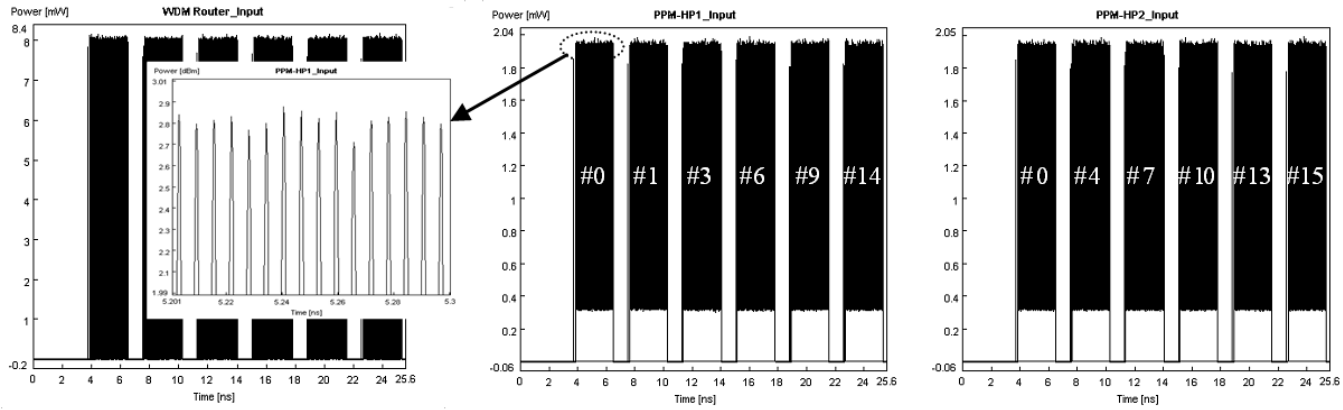
where $2^N \times T_s$ is the duration of a 2^N-slot PPM-frame, and $2T_b$ are the required processing time for the CEM module and the AND gate operation.

The time waveforms of six input WDM packets and their switched versions at the output ports are depicted in Figure 4. Figure 4(a) shows the multiplexed and demultiplexed packets waveforms at the input of the WDM router and PPM-HP1&2, respectively. Note that the intensity of the pulse stream is just above the minimum level. This is because of a very narrow pulse width (FWHM of 2 ps) overlapping within a bit period of 6.25 ps. This time overlap can be avoided by reducing the pulse width or the bit rate. As expected, packets are switched to their corresponding output ports according to the PPRT in Table 1. Packets at specific wavelengths observed at the outputs of the PPM-HP1&2 and the WDM ports are displayed in Figures 4(b), (c) and (d). The intensity overshot observed at the start of switched packets is due to the gain saturation of the SOA, in the OS module, when injected with a packet stream, where the proceeding bits will experience a lower amplification gain. This can be minimized by decreasing the optical power level of the input packet. There is also a small intensity fluctuation of less than 0.3 dB as shown in the insets of Figures 4(a) and (b). In [15] it is shown that regenerating of received packet streams with a larger intensity fluctuation may not be possible using a simple slicer with a fixed threshold level. The intensity fluctuation can be further reduced by applying a series of control pulses to the OS to keep the switching window wide open to allow the entire packet to go through. Note that in Figures 4(b), (c) and (d), packets with addresses #0 and #1 are switched to all outputs (i.e. broadcast) and multiple outputs (i.e. multicast), respectively.

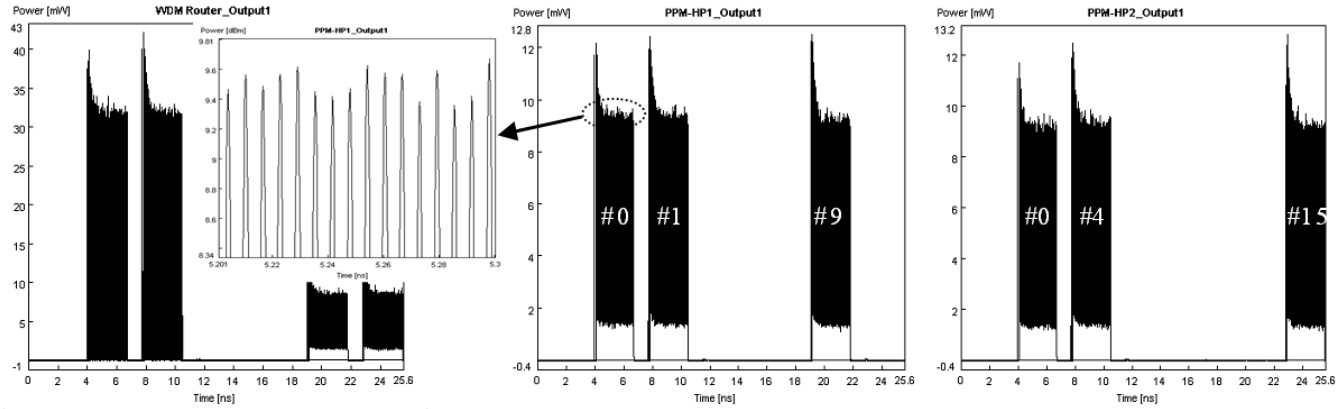
Inter-channel crosstalk (*CXT*) is an important issue in DWDM core networks that will result in transmission and node functionality impairment [16], and is defined as:

$$CXT = 10\log_{10}\left(E_{nt} / E_t\right), \quad (5)$$

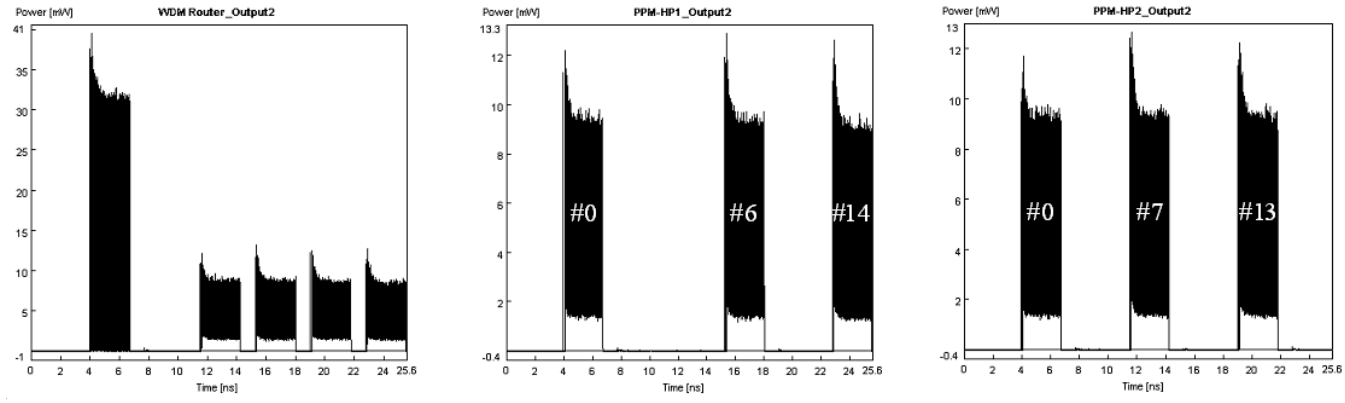
where E_{nt} is the output signal energy of all non-target channels (undesired wavelength) and E_t is the output signal energy of the target channel (desired wavelength). For evaluating the router *CXT* performance, two packets at λ_1 (packet 1 with address #4) and λ_2 (packet 2 with address #4) are sequentially applied to the input of the WDM router, see Figure 5. The *CXT* observed at the input and output1 ports of PPM-HP1&2 for a range of channel spacing $\Delta f = f_2 - f_1$ is depicted in Figure 6. The CXT_{output} level is constant at -27 dB for 0.4 THz < Δf < 1 THz and it increases exponentially when Δf < 0.4 THz. In the Δf range of 0.8 THz to 1 THz, CXT_{input} level is much lower than the CXT_{output} and increasing linearly for Δf < 0.8 THz. The minimum level of CXT_{output} is limited by the contrast ratio of the extracted clock signals from the CEM module [17]. Note that CXT_{output} is much lower than the CXT_{input} for 0.4 THz < Δf < 0.8 THz. The improvement in the crosstalk at the outputs of the PPM-HP is explained as follows: Signal emerging from the demultiplexer (i.e. the input signal of PPM-HP) at wavelengths other than the desired wavelength displays a very low input power level (< -0.5 dBm), thus as a result no matched signals


WDM Router_Input
PPM-HP1_Input
PPM-HP2_Input
#0 #1 #3 #6 #9 #14
#0 #4 #7 #10 #13 #15
Power [mW]
Time [ns]

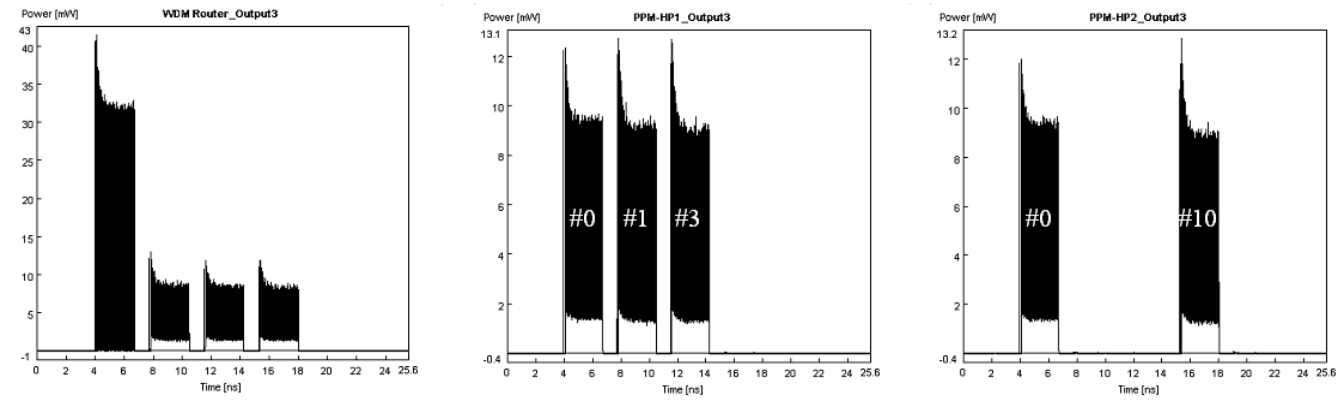
(a)


WDM Router_Output1
PPM-HP1_Output1
PPM-HP2_Output1
#0 #1 #9
#0 #4 #15
Power [mW]
Time [ns]

(b)


WDM Router_Output2
PPM-HP1_Output2
PPM-HP2_Output2
#0 #6 #14
#0 #7 #13
Power [mW]
Time [ns]

(c)


WDM Router_Output3
PPM-HP1_Output3
PPM-HP2_Output3
#0 #1 #3
#0 #10
Power [mW]
Time [ns]

(d)

Figure 4. (a) packets at the inputs of the WDM router and PPM-HP1&2 (the inset shows the power fluctuation observed at the input of PPM-HP1), (b) packets observed at the output 1 of the WDM router and PPM-HP1&2 (the inset shows the power fluctuation observed at the output 1 of PPM-HP1), (c) packets observed at the output 2 of the WDM router, PPM-HP1&2, and (d) packets observed at the output 3 of the WDM router and PPM-HP1&2

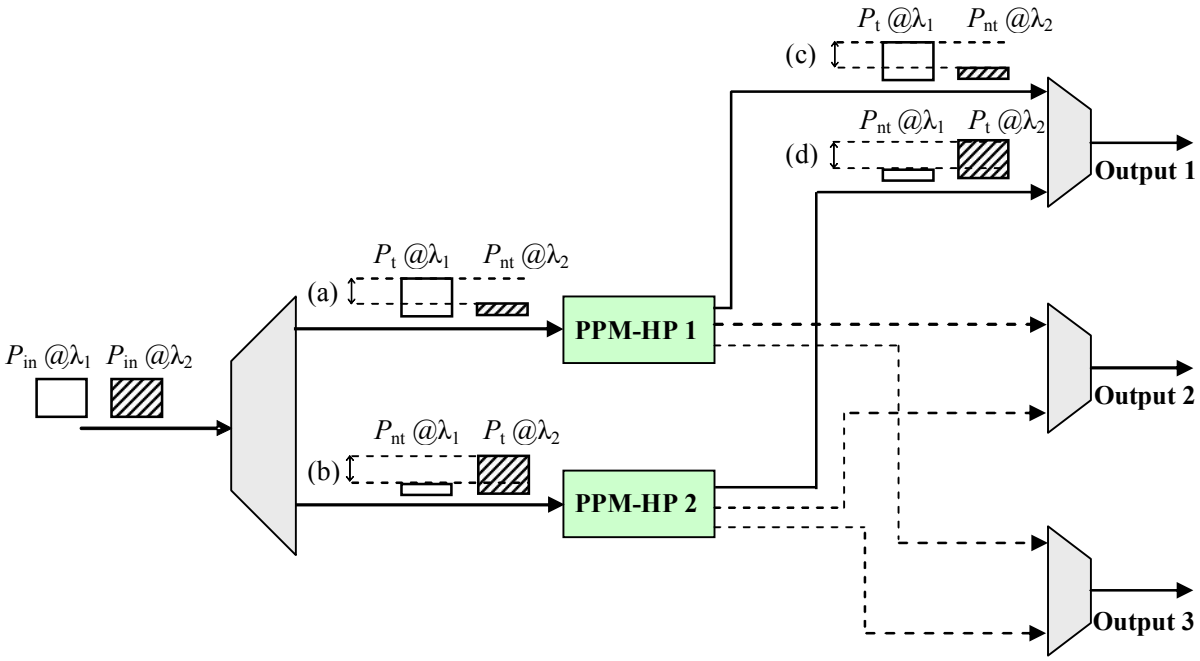


Figure 5. (a) The inter-channel *CXT* observed at input of PPM-HP1, (b) *CXT* observed at input of PPM-HP2, *CXT* observed at output1 of PPM-HP1, and (d) *CXT* observed at output1 of PPM-HP2

at the output of the AND gates. Therefore, a packet is directed to the non-target output port (i.e. the absorber port) of the optical switch.

The average optical power of packets observed at the output2 and the input of PPM-HP1 module is illustrated in Figure 7(a), showing a linear relationship with the input power up to 5.5 dBm, dropping at input power > 6.5 dBm. The average optical power at the output of the PPM-HP module increases with the average input power reaching a maximum level of ~16 mW (12 dBm). The gain observed is because of the gain of optical switches, see Figure 3. Note that in Figure 7(a) only the region one should be used. The drop in the average output power in PPM-Hp is mainly due to reduced power level of the extracted clock signals $c(t)$. This could be explained from Figure 7(b): The average output power of $c(t)$ increases with the average input power of the PPM-HP reaching a maximum levels of ~ 400 mW (25 dBm), and decreasing from the input power of > 5.5 dBm. The reduced average power level of the extracted clock signal is as a result of two-stage SMZ configuration employed in the CEM module [17]. Input packet stream with high power levels will results in high intensity control pulses within the CEM module, and consequently saturating the SOAs gain contained in CEM module, thus decreasing the output average power of the CEM module. For packets with a lower input power level, the extracted clock signal power level will be low, which in turn will result in reduced power level for the PPRT entries and the extracted PPM address bits. Consequently, the correlated output pulse signals as well as the packets at the output of the PPM-HP module will also experience reduced optical power levels.

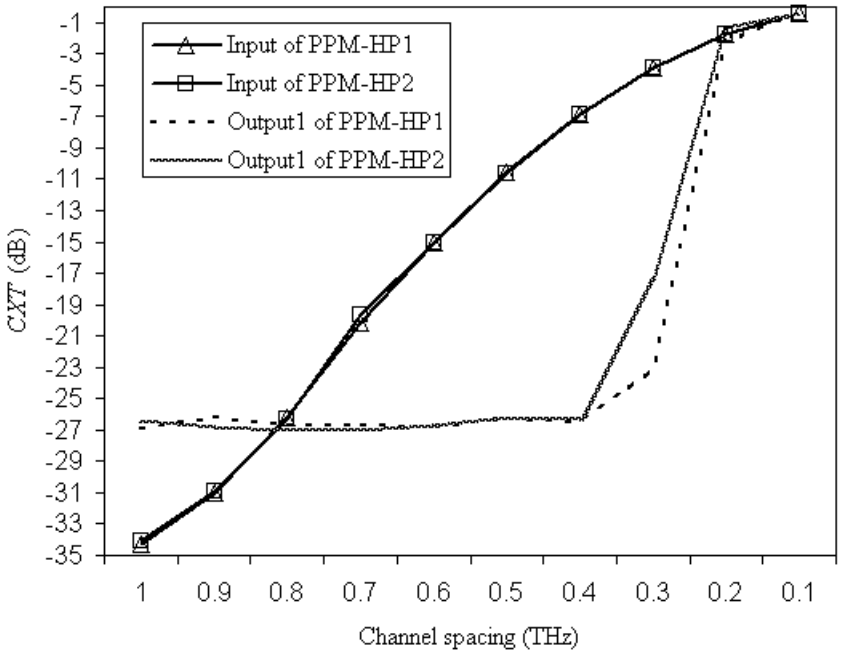
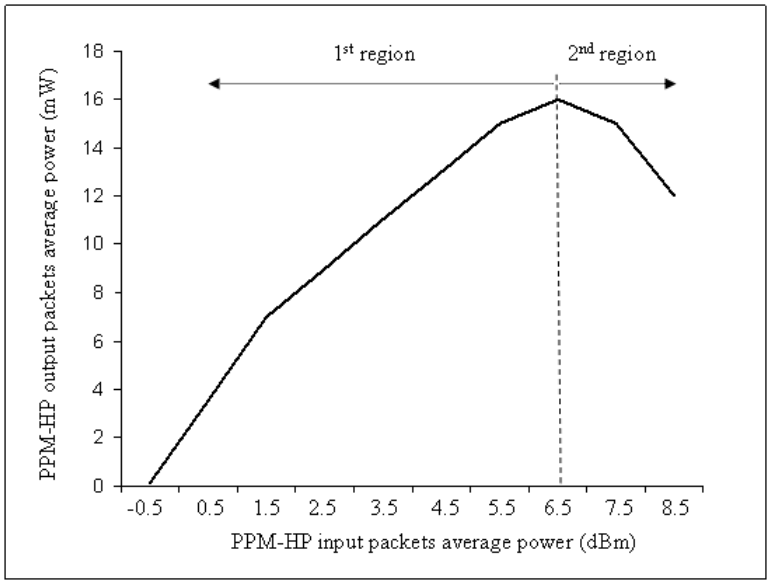
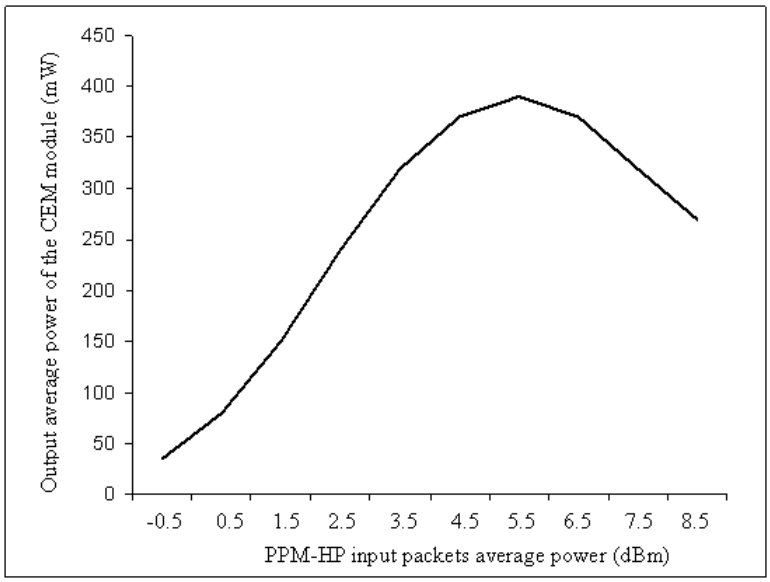


Figure 6. The channel crosstalk (*CXT*) observed at input of PPM-HP1&2 and output1 of PPM-HP1&2 against the channel spacing (the bandwidth of the WDM multiplexers and demultiplexer is 500 GHz)



(a)



(b)

Figure 7. PPM-HP input packets average power versus (a) PPM-HP output packets average power, and (b) output average power of the CEM module

5. CONCLUSIONS

The paper has presented an all-optical 1×*M* router architecture for a WDM core network. The PPM format adopted for the packet header address and the routing table entries offers fast correlation time and avoids the speed limitation imposed by the non-linear element based all-optical AND gates. Simulation results obtained illustrated that the proposed router can operate at 160 Gb/s with 0.3 dB of power fluctuations observed at the output ports and a channel *CXT* of ~ -27 dB when the channel spacing is greater than 0.4 THz and a demultiplexer bandwidth is 500 GHz. The output transfer function of the PPM-HP module showed that input packets with the average optical power levels less than 6.5 dBm should be used to ensure that switched packets at the output ports have higher average power and lower power overshoot.

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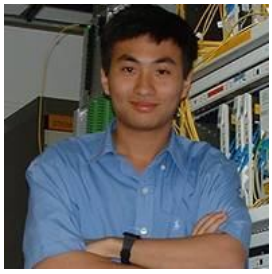

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